REMARKS/ARGUMENTS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1 and 3-20 are pending in the present application. Claims 1, 3, and 5 have been amended and Claim 2 has been cancelled without prejudice by the present amendment.

In the outstanding Office Action, Claims 1-20 were rejected under 35 U.S.C. § 103(a) as unpatentable over Sharma (U.S. Patent No. 6,910,169), Giles et al. (U.S. Patent No. 4,680,760, herein "Giles"), and Matsuda et al. (U.S. Patent No. 5,509,132, herein "Matsuda").

In light of the outstanding rejection on the merits, Claim 1 has been amended to recite the subject matter of Claim 2 and also that a first data pattern is corrected by an ECC circuit and is input to a BIST circuit. The claim amendments find support in Figure 3 and its corresponding description in the specification.

Briefly recapitulating, amended Claim 1 is directed to a semiconductor device that has a memory, an ECC circuit that has an error correction function of N bits for output data of the memory, and an error detection circuit configured to output a signal indicative of whether a total of an error bit number n1 detected by the ECC circuit when a first data pattern in testing target addresses of the memory is read out and an error bit number n2 detected by the ECC circuit when a second data pattern that is an inversion of the first data pattern in at least a part of the testing target addresses is read out exceeds N. The semiconductor device also includes a BIST circuit configured to read the first data pattern out of the testing target addresses of the memory as a first operation, write the second pattern in at least a part of the testing target addresses as a second operation, and read out the written second data pattern. The first data pattern is corrected by the ECC circuit and is input to the BIST circuit.

Turning to the applied art, Sharma discloses a semiconductor device including a memory and an ECC circuit. However, as recognized by the outstanding Office Action at page 5, second full paragraph, Sharma does not teach or suggest an error detection circuit having the claimed features.

In addition, Applicants respectfully submit that the ECC circuit of Sharma differs from the claimed ECC circuit for the following reasons. Sharma specifically discloses that a real data pattern, from which the inversed data pattern is created, is neither corrected by the ECC circuit nor input to a BIST circuit, as required by amended Claim 1.

The semiconductor device of Claim 1 advantageously achieves an accurate defect detection without increasing an area of a test circuit or a testing time by using the claimed BIST circuit.

To cure some deficiencies of Sharma, the outstanding Office Action relies on Giles for teaching the error detection circuit missing in Sharma and also for teaching a data pattern and inversed data pattern. However, Giles does not teach or suggest determining a first number of errors in the data pattern, a second number of errors in the inversed data pattern, and generating a signal if the sum of the first number and the second number exceeds a predetermined number N. In addition, Giles does not teach or suggest the features added to Claim 1 by the present amendment.

The outstanding Office Action relies on Matsuda for teaching that a signal is generated by a semiconductor device when a number of errors exceeds a predetermined number. However, Matsuda does not cure the deficiencies of Sharma and Giles discussed above. In addition, with reference to independent Claims 1 and 13, Matsuda does not teach or suggest that a sum of two different error numbers corresponding to a data pattern and an inverse data pattern are compared to a predetermined number in order to generate a signal.

Thus, Applicants respectfully submit that independent Claims 1 and 13, and each of the claims depending therefrom, patentably distinguish over Sharma, Giles, and Matsuda, either alone or in combination.

Consequently, in light of the above discussion and in view of the present amendment, the present application is believed to be in condition for allowance and an early and favorable action to that effect is respectfully submitted.

Respectfully submitted,

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